PVP 14

Code: EC5T3

III B.Tech - I Semester – Regular/Supplementary Examinations
October 2018

COMPUTER ARCHITECTURE AND ORGANIZATION
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) List the phases of the instruction cycle.
   b) Give one example each of logical and shift instructions.
   c) Draw the basic computer instruction formats.
   d) What do you mean by micro instruction and micro program?
   e) What is the purpose of using addressing modes in computers?
   f) What is serial communication ?
   g) What is DMA?
   h) What is the advantage of using 2's complement over 1's complement system?
   i) Perform 7-4 using 2's complement system.
   j) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline.
   k) Define parallel processing.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Draw the flow chart for instruction cycle. 8 M

   b) With a neat diagram explain bus and memory transfer. 8 M

3. a) Convert the expression Y= (P + Q) / (P – Q) into zero address, two address and three address instruction formats. 8 M

   b) Illustrate the concept of overlapped register windows for RISC processor. 8 M

4. a) Classify the interrupts that cause a break and explain them. 8 M

   b) What is the difference between isolated I/O and memory mapped I/O? What are the advantages and disadvantages of each? 8 M

5. a) Explain the Booth's Algorithm for multiplication of numbers (-9) and (-13) indicating all the steps involved, register values and their status at every step. 8 M

b) Draw the flow chart for floating point addition/subtraction representation. 8 M

6. a) Classify the array processors according to their internal organization. 8 M

b) Write short notes on i) pipelining ii) vector processing 8 M